

FIG. 1 (PRIOR ART)

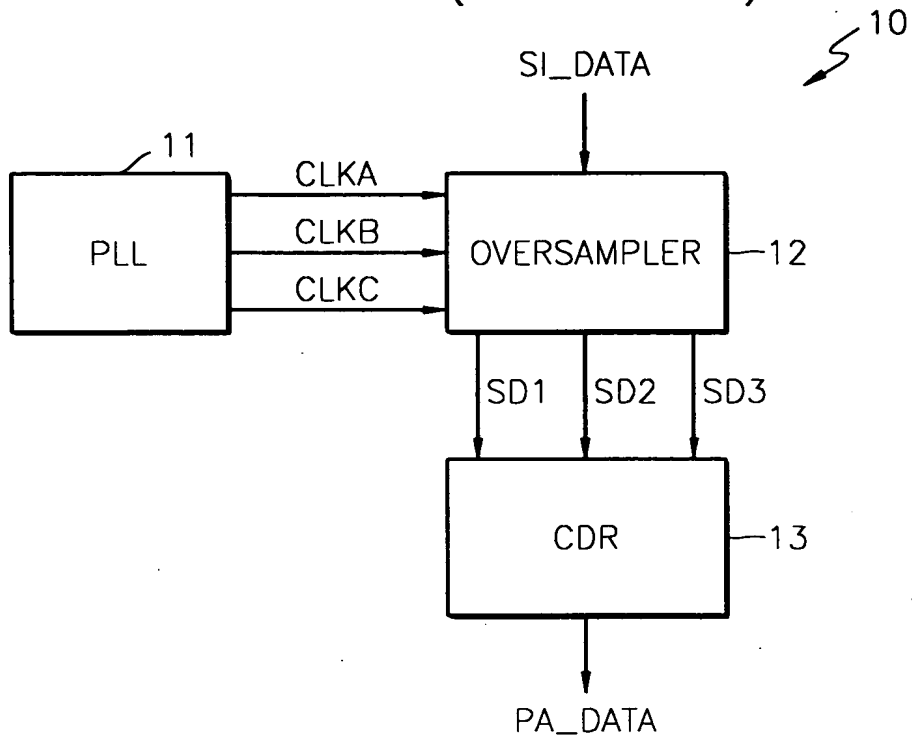


FIG. 2 (PRIOR ART)

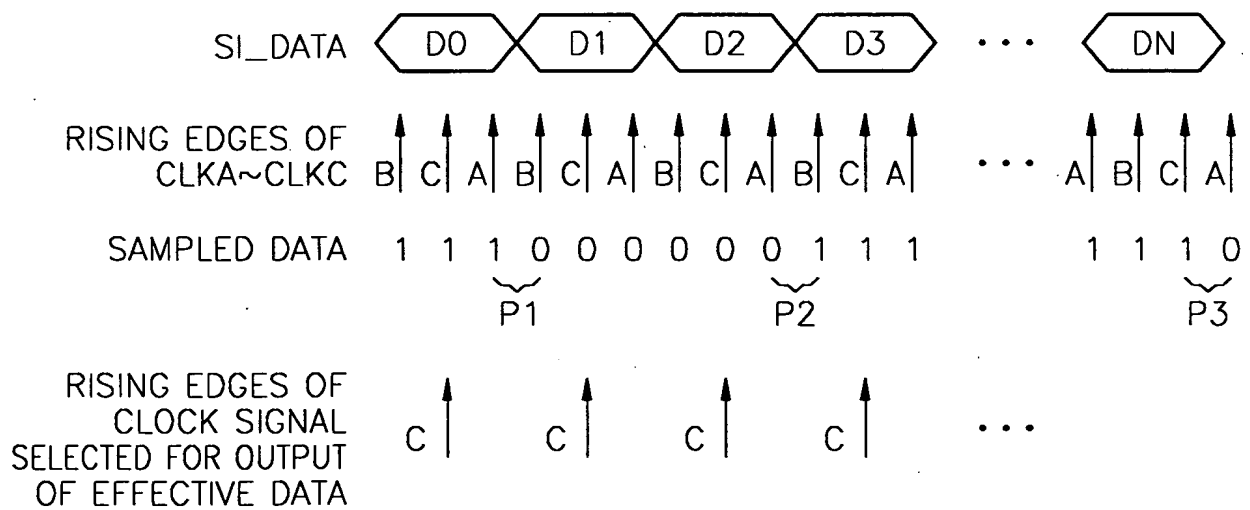


FIG. 3A (PRIOR ART)

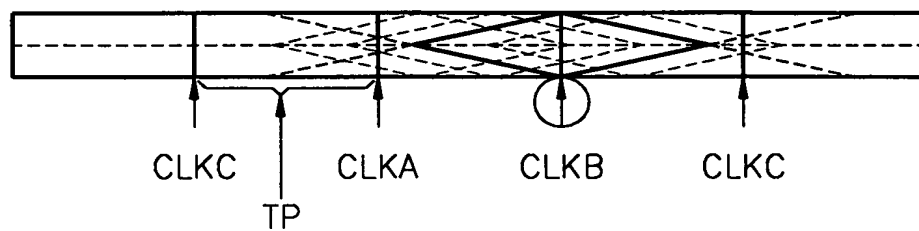


FIG. 3B (PRIOR ART)

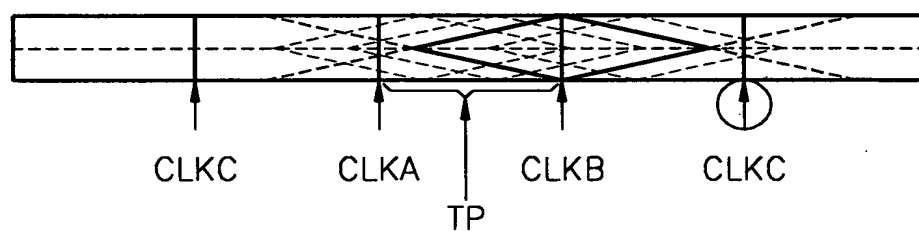


FIG. 3C (PRIOR ART)

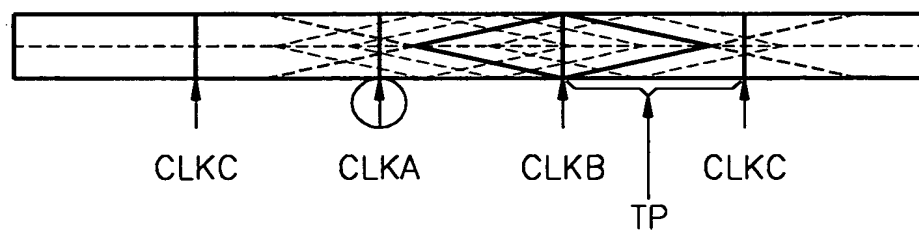


FIG. 4

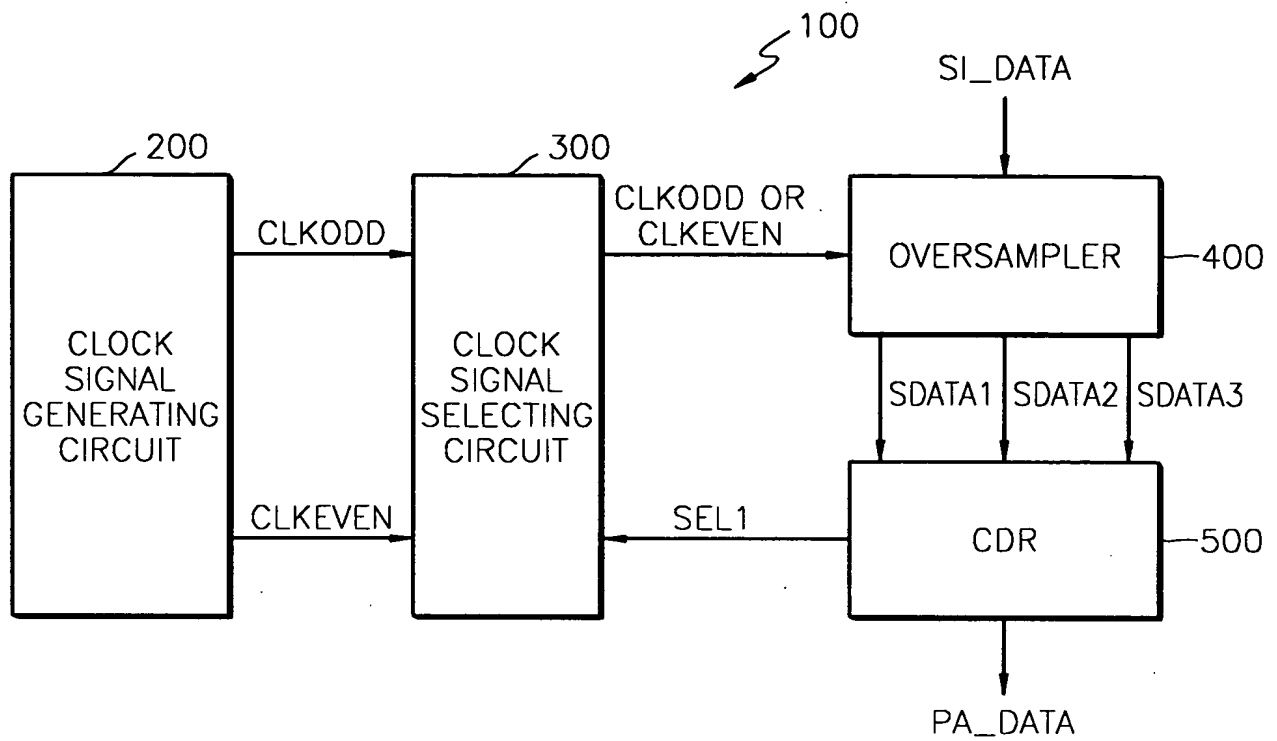


FIG. 5

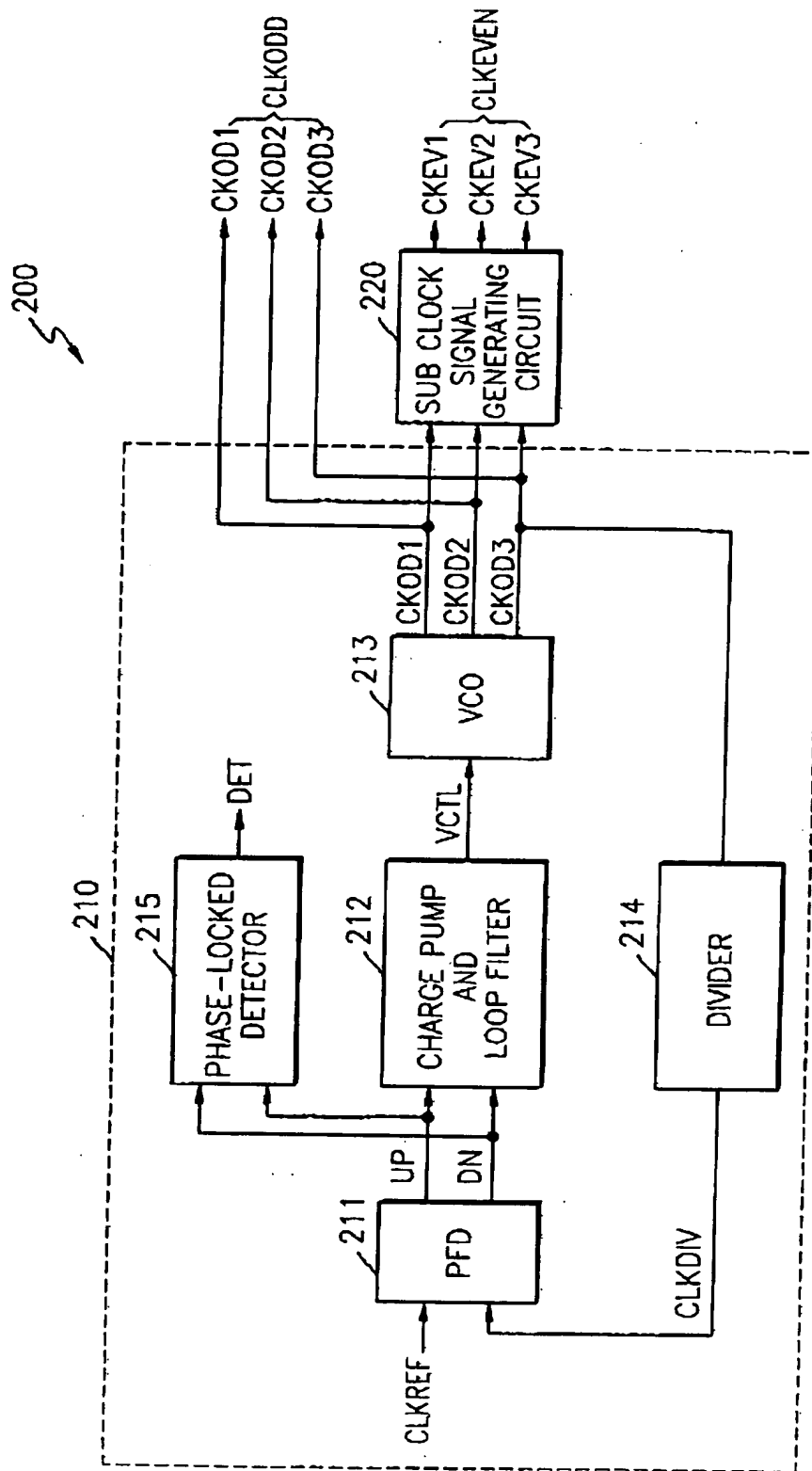


FIG. 6

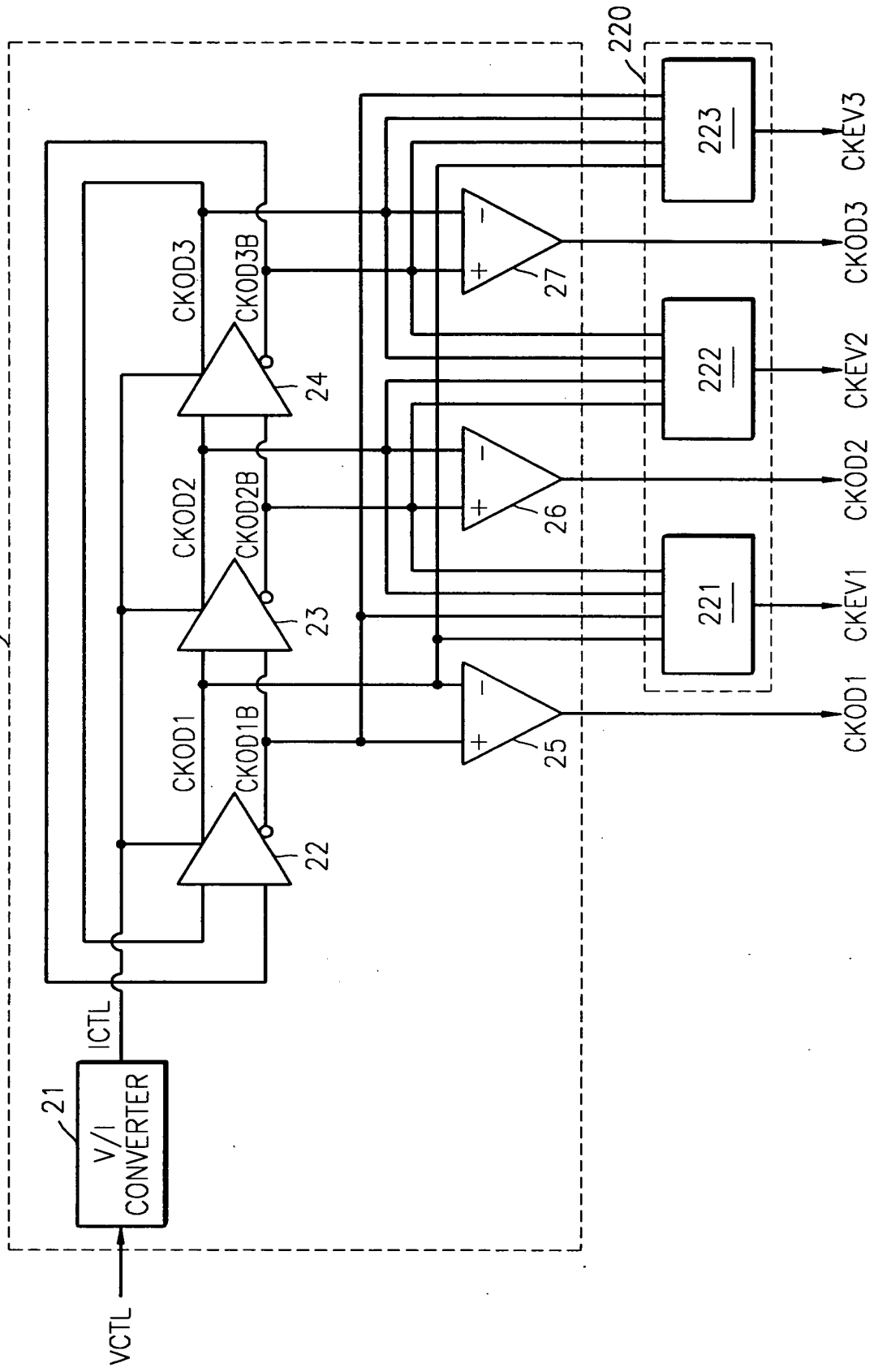


FIG. 7

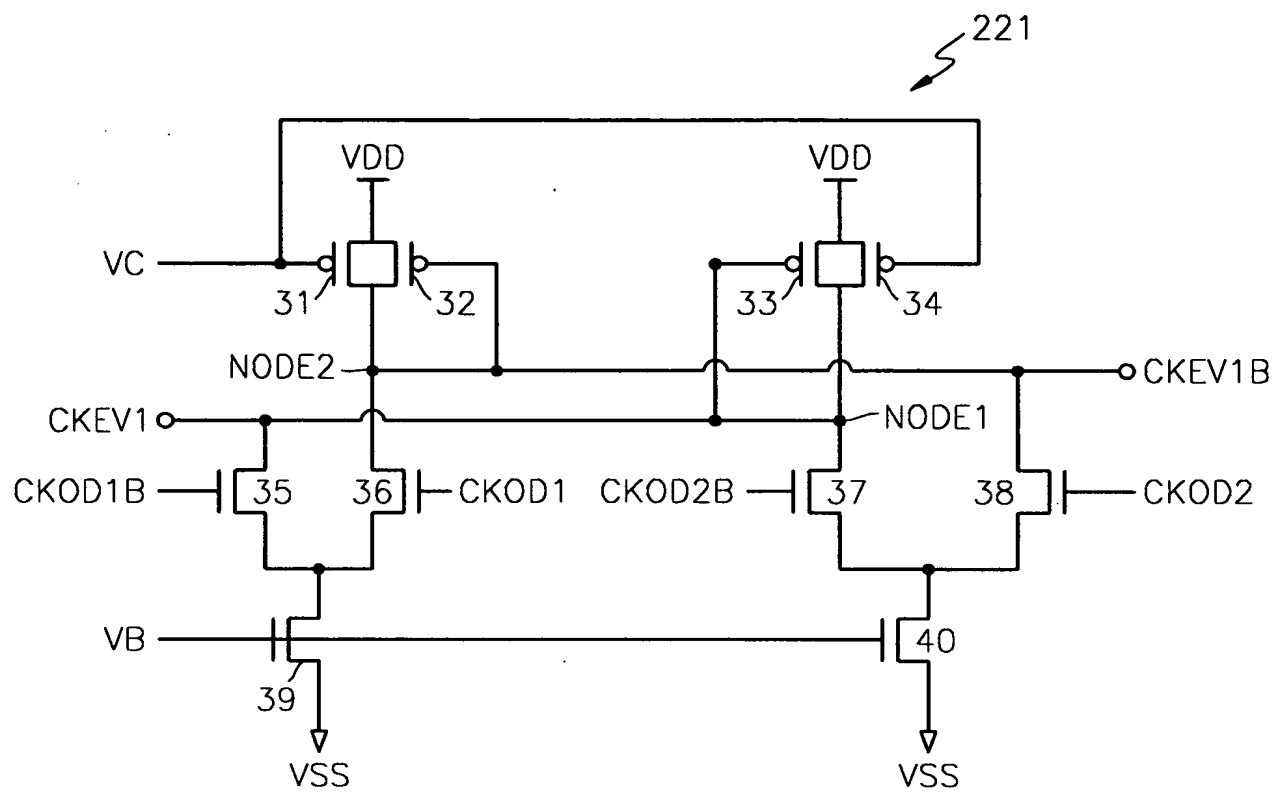


FIG. 8

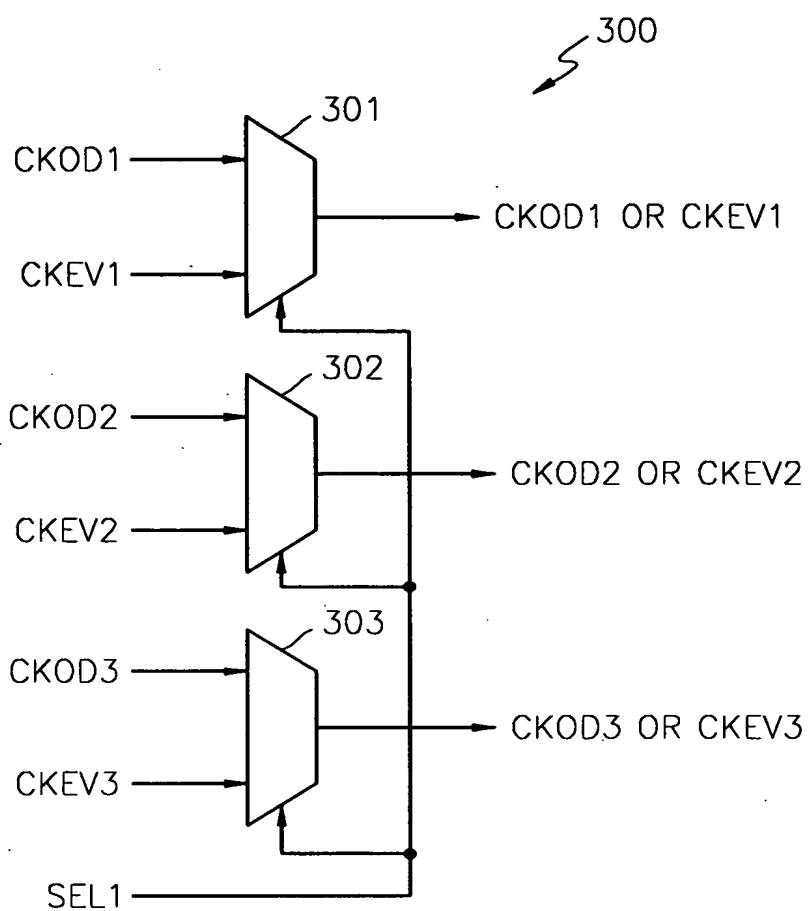


FIG. 9

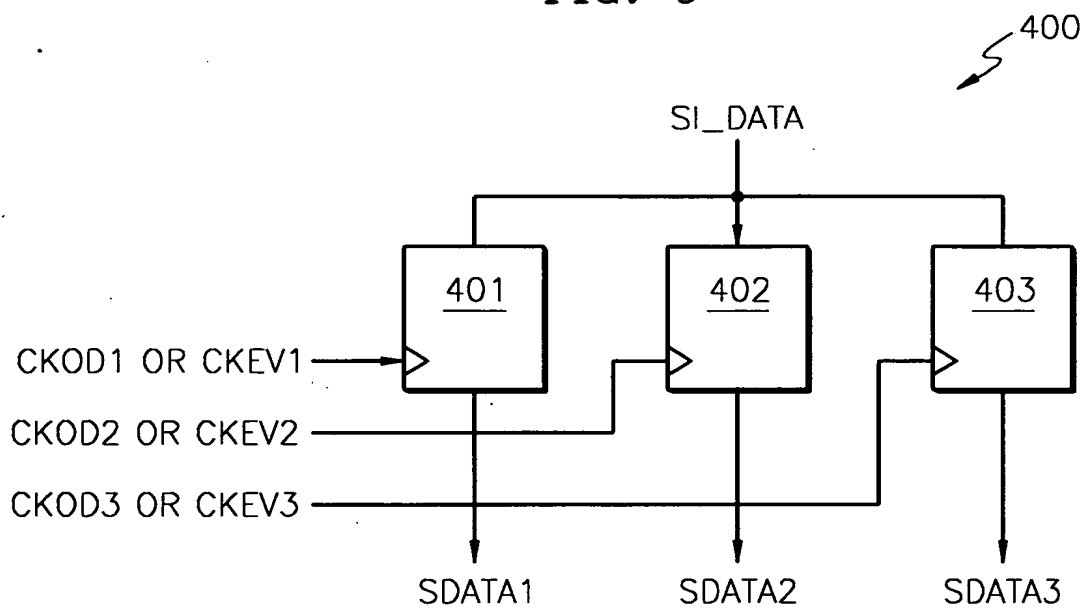


FIG. 10

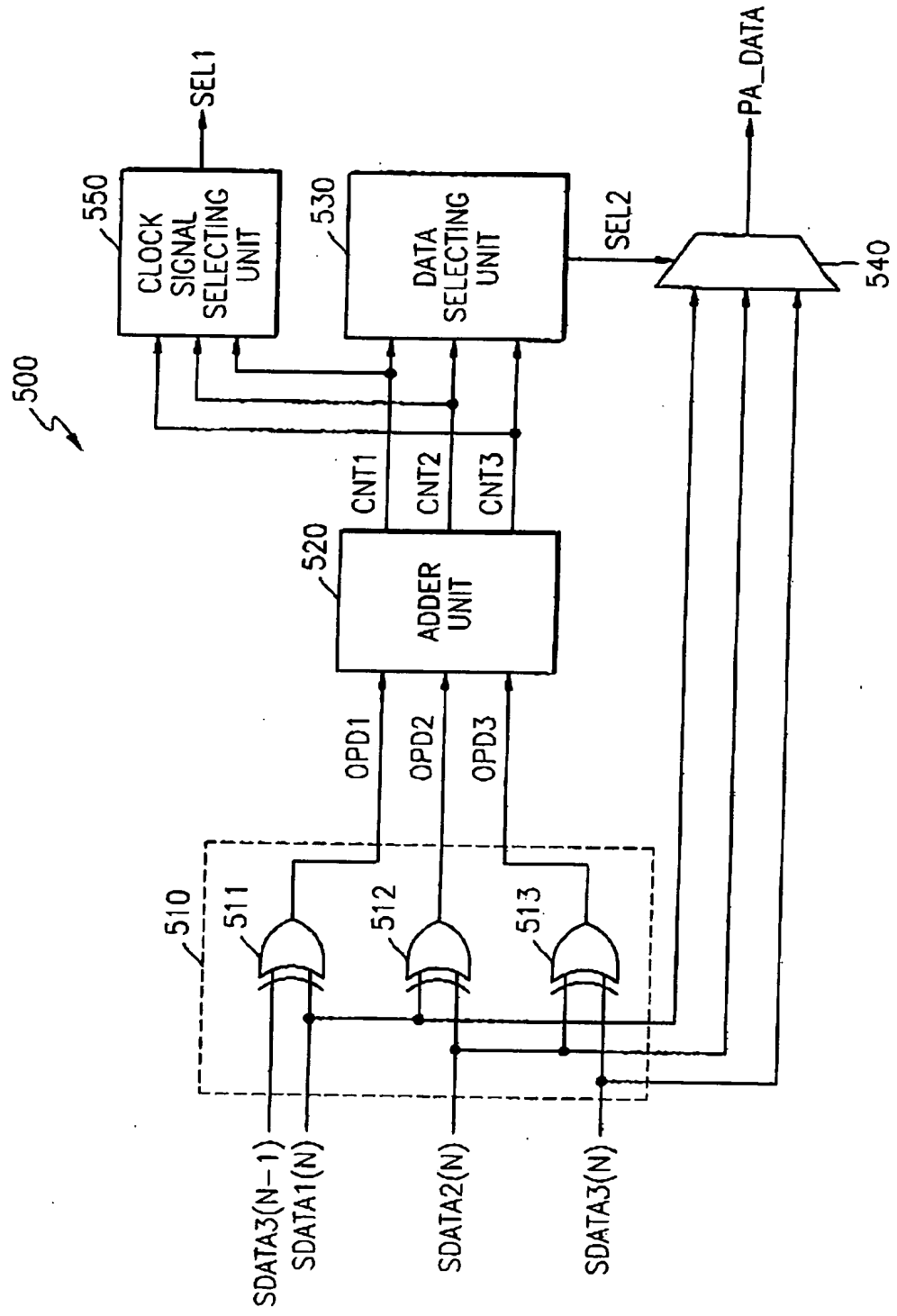
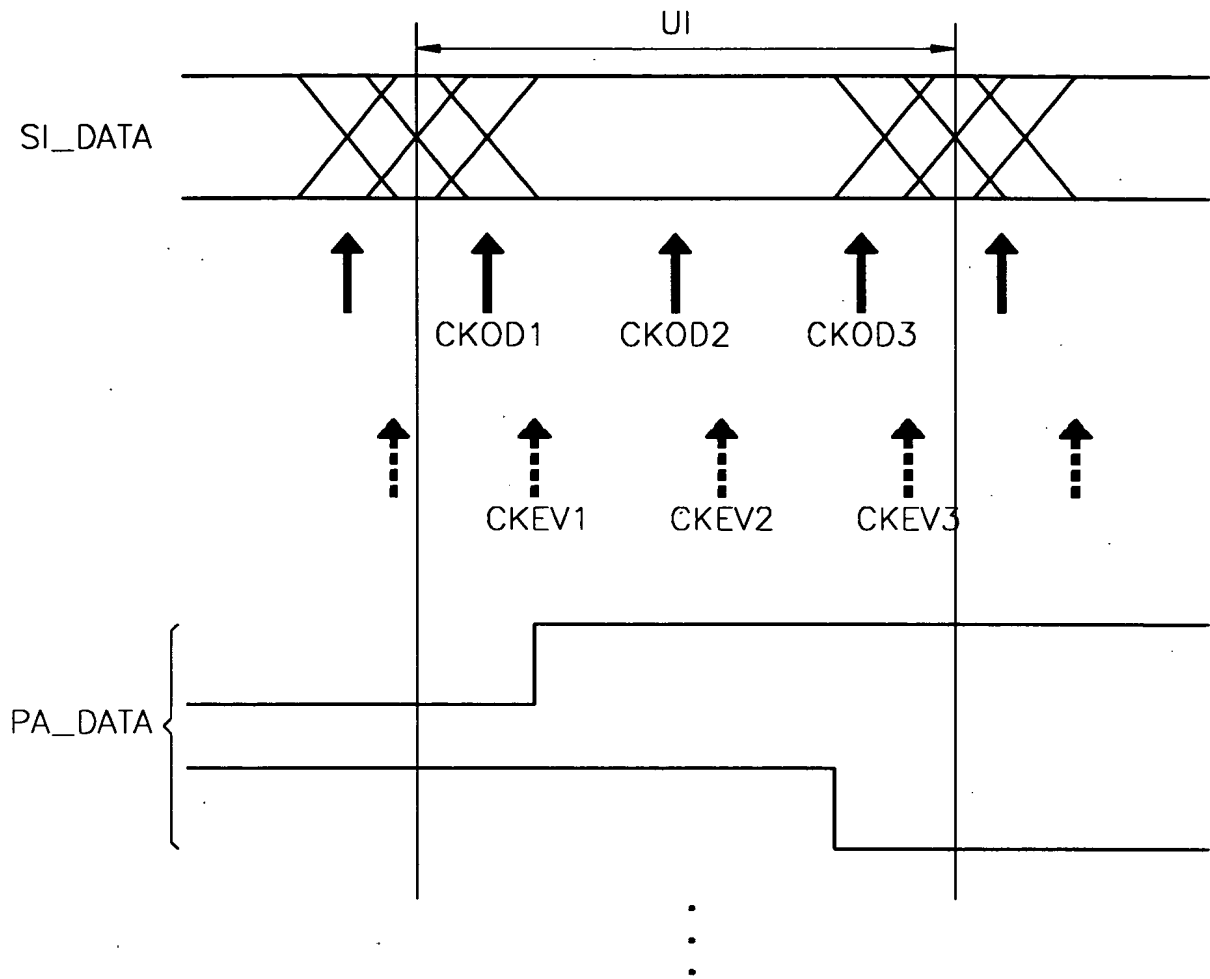


FIG. 11A



The diagram shows the timing relationship between SI_DATA and PA_DATA signals. The SI_DATA signal is a high-speed data stream with two segments of data (indicated by 'X' marks) separated by a period labeled 'UI'. The PA_DATA signal is a lower-speed signal that is active during the first segment of SI_DATA data. The PA_DATA signal is shown as a single line that is high during the first segment of SI_DATA data and low during the second segment. The PA_DATA signal is labeled with CKOD1, CKOD2, and CKOD3, which correspond to the first, second, and third clock cycles of the first segment of SI_DATA data. The PA_DATA signal is also labeled with CKEV1, CKEV2, and CKEV3, which correspond to the first, second, and third clock cycles of the second segment of SI_DATA data. The PA_DATA signal is shown as a single line that is high during the first segment of SI_DATA data and low during the second segment. The PA_DATA signal is labeled with CKOD1, CKOD2, and CKOD3, which correspond to the first, second, and third clock cycles of the first segment of SI_DATA data. The PA_DATA signal is also labeled with CKEV1, CKEV2, and CKEV3, which correspond to the first, second, and third clock cycles of the second segment of SI_DATA data.

FIG. 12

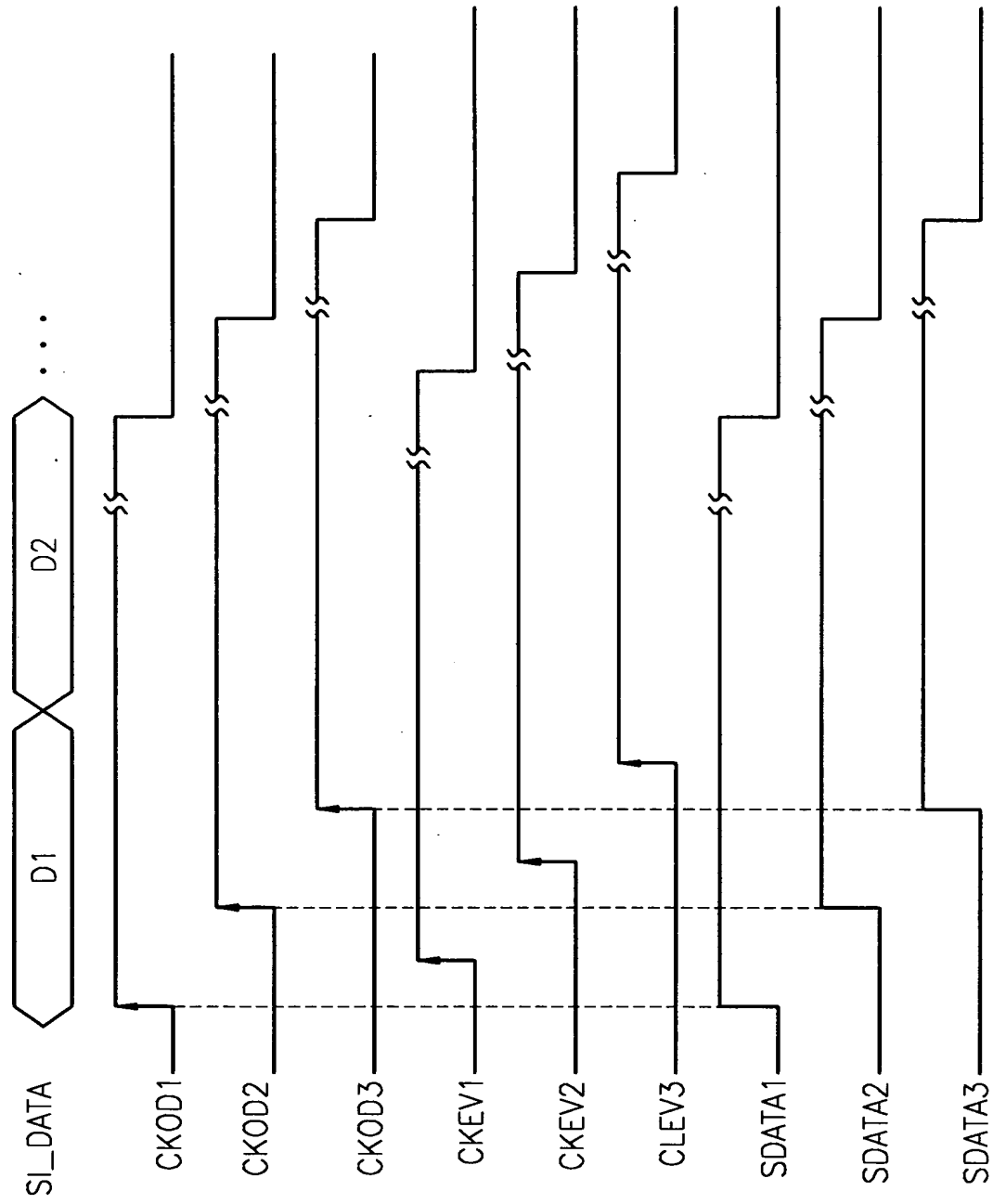


FIG. 13

